**Algorithm for outputting 32MHz clock from DIO5 of transceiver to MCU:**

NOTE 1: The transceiver takes in the actual XTAL connected on pins XTA (47) and XTB(45) at the startup time

NOTE 2: CLKOUT (DIO5) is controlled through RegDioMapping2

NOTE 3: If ClkOut is used to drive the external clock source to the MCU, EXTAL (PTA18) is not

available as GPIO.

* 1. Immediately after reset, DIOs are configured as **Outputs ( that means we don’t have to set them as outputs)**
  2. Map RegDioMapping2 –address 0x26
  3. Select clock out frequency (Pg. 115)
  4. Port Memory Space given in 115 to set RegDioMapping2
  5. The ClkOut functionality is controlled by programming transceiver Register RegDioMapping2 (0x26) (see Section 7.10, “IRQ and Pin Mapping Registers”):

1. Access the address byte of REgDioMapping2 : 0x26
   1. Write the appropriate value (000-111) on the bits 0-2 to get appropriate clock frequency output ( Refer to page #47 in **MKW01xx Reference Manual)**

**NOTE: DIO5 is mapped to Clkout by default (00 is the default value of DIO5)**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Value |  |  |  |  |  | 0 | 0 | 0 |
| Bits | 7 | 6 | 5 | 4 | 3 | **2** | **1** | **0** |

The values are as follows (pg #115)

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 111 | 110 | 101 | 100 | 011 | 010 | 001 | 000 |
| Off | 62.5K | 1M | 2M | 4M | 8M | 16M | 32MHz |

**# Enabling External Reference Clock mode in MCU**

1. Enable using the oscillator circuits by setting the external reference clock selection bit. (pg .502)
   1. Access OSC control register at 0x4006\_5000 base + 0x0h offset =0x4006\_5000
   2. Set bit 7 high

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Value | 1 |  |  |  |  |  |  |  |
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

1. Request for External Reference clock by clearing bit 2 in MCG\_C2 register (pg:464)
   1. Address: 4006\_4000h base + 1h offset = 4006\_4001h

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Value |  |  |  |  |  | 0 |  |  |
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

/\* Not needed if already in superviser mode \*/

1. In user mode, for MCG, RCM, SIM (slot 71 and 72), SMC, LLWU, and PMC, reads are allowed, but writes are blocked and generate bus error.(pg 218). So, first get write access for non-supervisor mode: (pg 685)
   1. Access RTC\_CR Register:

4003\_D000h base + 10h offset = 4003\_D010h

* 1. Set bit 2

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 1 |  |  |
| 31 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 2 | 1 | 0 |

1. Set PLL Engaged External Mode (PEE-mode)

NOTE: **In PEE mode, the MCGOUTCLK is derived from the output of PLL** **which is controlled by an external reference clock. The PLL clock frequency locks to a multiplication factor, as specified by its corresponding VDIV, times the selected PLL reference frequency, as specified by its corresponding PRDIV. The PLL's programmable reference divider must be configured to produce a valid PLL reference clock. (pg: 478)**

* 1. When C1[IREFS] is set, the external reference clock will not be used by the FLL or PLL. So clear it.
     1. Access MCG\_C1 register: 4006\_4000h base + 0h offset = 4006\_4000h
     2. Set bits 7-6 to 00 to select the output of PLL

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Value | 0 | 0 |  |  |  |  |  |  |
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

* 1. Select Reference clock source to external
     1. Access MCG\_C1 register: 4006\_4000h base + 0h offset = 4006\_4000h
     2. 0 is written to C1[IREFS] which is bit 2.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Value |  |  |  |  |  | 0 |  |  |
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

* 1. Select the multiplication factor VDIV – Select the amount to divide the VCO (voltage controlled oscillator) output of the PLL.
     1. MCG\_C6 Address: 4006\_4000h base + 5h offset = 4006\_4005h
     2. Multiply by 32 (01000) Options given in (pg: 469)

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Value |  |  |  |  |  |  |  |  |
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

* 1. Select PRDIV value
     1. MCG\_C5 Address: 4006\_4000h base + 4h offset = 4006\_4004h
     2. We’ll have to write an appropriate value? ? Options given in (pg: 467)

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Value |  |  |  |  |  |  |  |  |
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

* 1. Select PLL as an output (choose between PLL and FLL)
     1. Access MCG\_C6 register: Address: 4006\_4000h base + 5h offset = 4006\_4005h
     2. Set bit 6

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Value |  | 1 |  |  |  |  |  |  |
| Bits | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

After all these steps, we get **MCGOUTCLK == EXTL clock frequency**

1. Channel EXTL clock frequency to the core
   1. Set OUTDIV1 value to 1
      1. Access System Clock Divider Register 1 (SIM\_CLKDIV1) : 4004\_7000h base + 1044h offset = 4004\_8044h
      2. Set bits 31-28 to 0000 (pg. 296)

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 31 | 30 | 29 | 28 | 27 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | 0 |